REMARKS

Claims 1-36 are pending. Claims 1 and 30 are independent.

The examiner rejected claims 1-29 under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement.

The examiner also rejected claims 1-29 under 35 U.S.C. §112, second paragraph, for being indefinite.

Applicant has amended claims 1-29 to recite "(a) method of operating a multithreaded processor comprising." No new matter has been added.

Accordingly, claims 1-29 are proper under 35 U.S.C. §112, first and second paragraphs.

The examiner continues to use Agarwal to reject claims 1-23, 26 and 30-36 as having been anticipated.

Applicant's claims 1 and 30, as amended, recite "directing the processor having a plurality of threads executing in a plurality of microengines to issue a memory reference to an address in a memory shared among threads executing in the microengines while a context of a thread is waiting," or similar language. Agarwal neither describes nor suggests at least this quoted claim feature.

Agarwal neither describes nor suggests a processor having a plurality of threads executing in a plurality of microengines. The examiner argues that this claimed feature is disclosed in Agarwal at Sections 2 and 3. But applicant fails to see where in Agarwal this is disclosed or suggested.

Agarwal discloses a system referred to as ALEWIFE. (Agrawal, page 105, section 2) ALEWIFE includes nodes. Applicant's claimed invention does not involve nodes.

Each of the ALEWIFE nodes is connected via a direct, packet-switched network. (Agrawal, page 105, section 2.1) Applicant's claimed invention does not involve connections of nodes via a packet-switched network.

Agarwal discloses, as admitted by the examiner, that each node includes a processing element, floating point unit, cache, main memory, cache directory controller and a network

switch (Agrawal, page 105, section 2.1) No plurality of threads executing in a plurality of microengines is described or suggested.

Agarwal discloses a controller in a single ALEWIFE node that synthesizes a global shared memory space via messages to other nodes, and satisfies requests from other nodes directed to its local memory. (Agrawal, page 105, section 2.1) Thus, Agarwal discloses the exact opposite of applicant's claimed invention, which includes directing the processor having a plurality of threads executing in a plurality of microengines to issue a memory reference to an address in a memory shared among threads executing in the microengines.

Agarwal discloses a network used to satisfy requests:

> **In the ALEWIFE system, a context switch occurs whenever the network must be used to satisfy a request, or a failed synchronization attempt. (Agarwal, page 105, section 2.1, paragraph 4)**

No where in applicant's claims is a "network" shown.

Agarwal is very different from applicant's claimed invention. Agarwal, unlike applicant's claimed invention, is concerned with the large latencies associated with cache misses that require network access. (Agarwal, page 107, lines 1-2) Agarwal performs context switching in a node when a remote request (outside of the node) comes into the node's local memory. Thus, Agarwal is addressing a completely different problem than applicant's claimed invention.

Accordingly, claims 1 and 30 cannot be anticipated by Agarwal.

The examiner continues to use Agrawal to reject dependent claims 24, 25 and 27-29 as having been obvious.

Applicant respectfully disagrees. Claim 1 recites "directing the processor having a plurality of threads executing in a plurality of microengines to issue a memory reference to an address in a memory shared among threads executing in the microengines while a context of a thread is waiting." Agarwal does not teach or suggest this quoted claim feature, as discussed above. One skilled in this art would not be drawn to Agarwal since Agarwal teaches a solution to a problem that is the very opposite to applicant's claimed invention. More specifically, as applicant described above, Agarwal teaches a first node with a local memory waiting while a second node accesses the local memory of the first node. Applicant's claimed invention issues a

memory reference to an address in a memory shared among threads executing in the microengines. Accordingly, claim 1 is not rendered obvious by Agarwal.

Claims 24, 25 and 27-29 depend upon, and add further limitations, to claim 1. Accordingly, claims 24, 25 and 27-29 are not rendered obvious by Agarwal.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: June 7, 2005

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